International Journal of Research in Advent Technology, Vol.6, No.6, June 2018
E-ISSN: 2321-9637
Available online at www.ijrat.org

Optimized Design and Simulation of 4-Bit Johnson Ring Counter Using 90nm Technology

Abhishek Rai[1], Rajesh Mehra[2]
Electronics and Communication Engineering Department[1, 2], ME Scholar[1], Associate Professor[2]
National Institute of Technical Teacher Training and Research, sector-26, Chandigarh[1, 2]
Rai199424@gmail.com[1]

Abstract — Sequential circuits have vital role in the designing of digital system. Sequential circuit design with high speed and low power at smaller chip size has become the major concern for researcher and day by day development in VLSI technologies sustain the flow for achieving the desired goals too. Counter is a sequential circuit which have various applications in the field of embedded system, pattern generations, signal synthesis, Digital to Analog conversion etc. In this paper, a designing escalation mechanism has been deployed to design a high speed, cost effective and low power 4-bit Johnson ring counter which can also be used for higher order ring counter designs. In this work, performance of the expected ring counter is boost by using a negative edge triggered D flip-flop which has 10 MOS transistors in its design as compare to conventional counter. The proposed paper has accomplished the design goals by reducing the power consumption and area of counter.

Keywords — Ring counter; D flip flop; negative Edge trigged; VLSI power dissipation; CMOS gates

1. INTRODUCTION

In digital circuits,counter plays very vital role. Counters are digital circuits which follow a particular pattern in response to the number of times an event happened. So every time whenever a clock comes, present state of counter changes to next state. This creates its broad applications in digital control systems, embedded systems, processors, memories, frequency synthesizer, digital timing circuits etc. [1]. A counter consists of set of flip flop which stores bits „0" and „1" and results in counter state pattern. The capabilities of a counter can be represented by the maximum number of states in a counter.

In sequential circuits, ring counter has made its place in controlling application based on its unique counting sequence. It uses a shift register in which set of flip flop are cascaded to circulate a bit „1" through all the flip flops. Therefore, inputs of flip flops are derived from the output of previous flip flop. In case of first flip flop, the output of last stage is given back to first stage. Initially, first stage is required to be set by external input „pre-set" and other flip flops are cleared. So for 4-bit Johnson ring counter, we start with 1000 binary pattern and then 1 circulate as 1100, 1110, 1111 and then again to 1000 binary pattern in next 4 input clock pulses [2].

The increment in manufacturing capabilities of VLSI industries has expanded the technical world. A CMOS inverter is basic cell in VLSI design. Transistor count is increasing day by day which leads to reduce the chip size, increase its speed and reduce its power consumption and chip size [3]. But quest of mobility, tiny product size, and more battery back-up is creating a vacancy for more enhancements in VLSI design parameters. So selection of better technology and less number of CMOS logic gates make design more power efficient and effective for digital designing. In this paper, design ofJohnson ring counter is proposed using D flip-flop

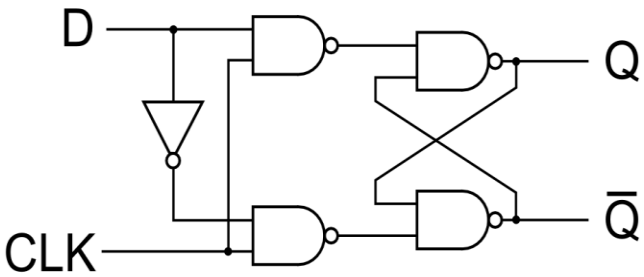


Fig.1. D flip-flop using NAND Gate

And a comparison of this circuit has been done with its conventional design in terms of speed and power dissipation. For better design, negative edge trigged clock circuit is employed in the D flip-flop.

Table1. Truth table of D flip-flop

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

In this work, micro-wind tool is used for the designing of Proposed counter. The work in this paper proceeds as:
Section 2 explains the designing aspects of the CMOS circuit utilization. Section 3 describes the design of Ring counter circuit. Section 4 presents the recommended schematic design of counter.The simulations and the results of proposed work are discussed in 5 section and in the section 6, the paper is concluded.

2. DESIGNING ASPECTS

In VLSI circuit design, main motive is to minimize the power consumption for CMOS circuits. In VLSI applications, the use of continuously increasing clock frequency is the main cause of increasing the power consumption in CMOS circuit design even the circuit operates at low supply voltage. In CMOS design, Power consumption has a static component resulting from consisting of threshold conduction through inactive transistors, leakage of inactive device, contention current and gate tunnelling current etc. In VLSI designing the other motive is to reduce the area of our design by using different polysilicon and metal materials. We can also increase the speed of operation by reduced the area of our design with the help of different designing tools. We use different designing tools like DSCH and microwind for the implementation of our VLSI circuit.CMOS designing is done by different P-MOS and N-MOS, during designing of our VLSI circuit we use different layout design like semi-custom or fully custom to reduce the area and power our design. During designing of 4-bit Johnson ring counter we use four D flip-flop of negative edge triggered in DSCH and for making one D-flip-flop we use four nand gate and one inverter. During designing we have to strictly follow lambda rules if we violate lambda rules design error should occur and area and power get increased.

3. RING COUNTER

Ring counter is like round move enrol. A particular pattern is follow and it is a synchronous counter, clock is given to all the flip-flop simultaneously. Ring counter should work on high frequency operation. Clock time period in Ring counter not depend on the number of bits, its only depend on the propagation delay of the flip-flop. The yield of the last flip-flops nourished to the contribution of the primary flip-tumble. There are two sorts of ring counters: (I) straight ring counter or Over beck counter interfaces the yield of the last flip-tumble to the principal flip - slump input and courses a solitary one (or zero) piece around the ring. For instance, in a 4-enlist one-hot counter, with introductory enrol estimations of 1000, the rehashing design is: 1000, 0100, 0010, 0001, 1000... . .

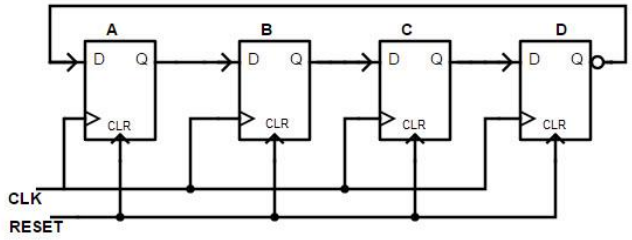


Fig.2. Synchronous Ring counter

3.1 A contorted ring counter, likewise called Johnson counterinterfaces the supplement of the yield of the last flip-flop to the contribution of the principal flip-tumble and circles a flood of one's trailed by zeros around the ring. For instance, in a 4register counter, with beginning register estimations of 0000, the rehashing design is: 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000...

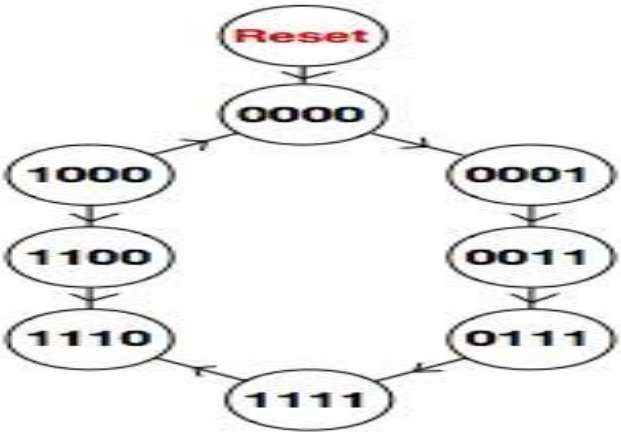


Fig.3. State representation of Johnson counters

[4]. Ring counters are utilized as a part of equipment rationale plan (e.g. ASIC and FPGA) to make confused limited state machines. Ring counters are utilized to encode contribution to different structures like decimal, octal and parallel and so on. Once a check beat is initiated in these counters, just a single of the FFs is "set", as only one piece "1" would turn in the circuit [5]. An n- bit synchronous ring counter is built up by cascading n D flip- flops in a chain by synchronizing the flip- flops with the same clock and setting the first flip- flop to status.

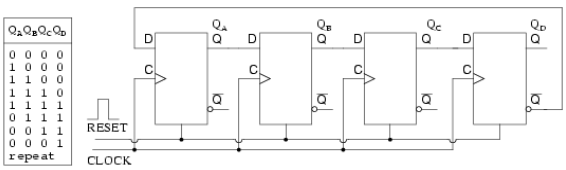


Fig.4. Four Bit Johnson Ring Counter

In DSCH We design 4 Bit Johnson Ring counter as shown below

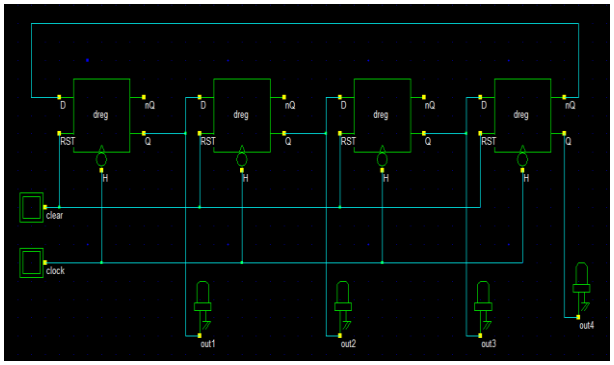


Fig.5. 4-Bit Johnson Ring Counter in DSCH

4. Layout Design Simulation

To start with we create Verilog document of our ring counter in DSCH. Presently this verilog document is gathered in microwind and an auto produced design is made. We can Choose diverse foundries which we have accessible in the library of Microwind programming. Here the chosen foundry is 90 nm. This auto produced design is spoken to in Figure2

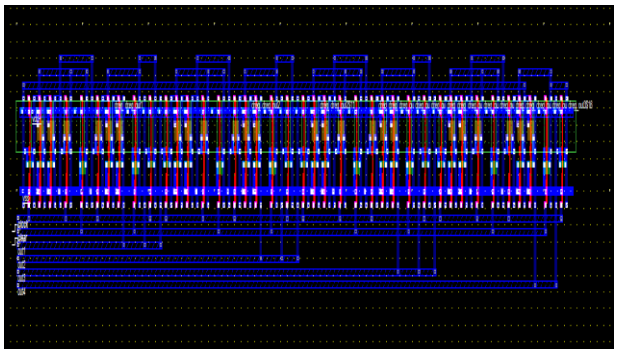


Fig.6. Fully automatic layout design

Check this layout for DRC and if there is no error presentin the layout, the layout is simulated. Also, check the simulation output and if the output matches the output of the 4-bit Johnson ring counter, we further check the area and the power of this auto generated layout of 4-bit Johnson ring counter. Figure 3 shows the output of the 4-bit Johnson ring counter. Power can also be measured from the result of simulation.

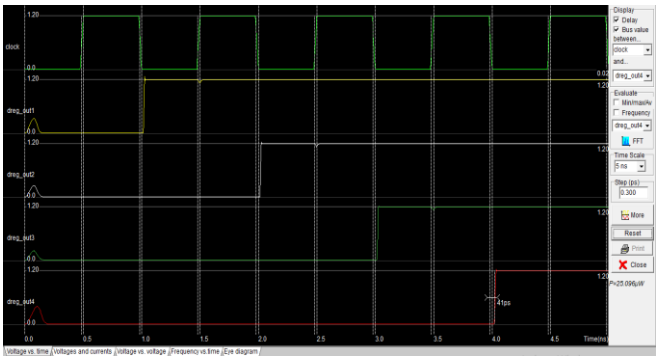


Fig.7. Auto Generated 4-bit Johnson ring counter output

The power measured here is 25.096µW. The consumed Area here is 297.5µm^2.
Now in second step we directly use in-built transistors the process being known as semi-custom layout design. In this method developer makes the connections and hence there is a huge possibility that area of layout design may reduce. A D flip- flop is constructed using the semi-custom layout of P- MOS and N- MOS [8]. Only ten transistors were used to make the design of D type flip flop. Thus this design can be much more Area Efficient than auto generated layout. Figure4represents the layout using the semi-costumed transistors i.e. N- MOS and P- MOS.

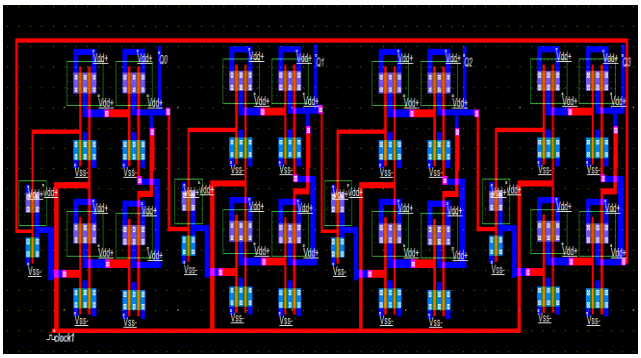


Fig.8.Semi-Custom Layout of 4- bit Johnson Ring Counter

At the point when the design is prepared it is again checked for DRC and if there is no blunder introduce in the format, the circuit is reproduced and the yields are acquired. The acquired yield is checked with reality table of 4-bit Johnson ring counter. In the event that reality table is confirmed we can additionally check the power and territory devoured by this second technique. Figure 5 demonstrates the yield acquired by re-enacting the above circuit.

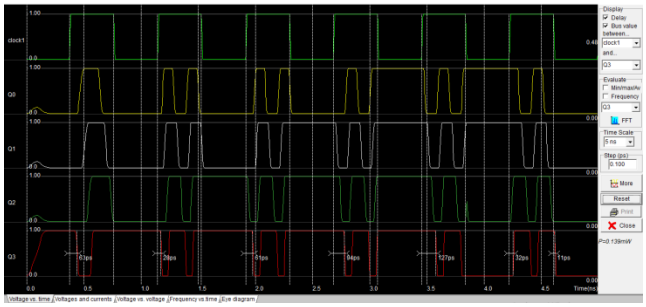


Fig.9. Semi-custom timing Diagram

Here the power consumed is 0.139 mw. The areaConsumed by this layout is 195.0 μm^2using semi-custom layouts.

5. RESULT DISCUSSIONS

Here the comparison between the auto-generated and semi-custom layout design should be done with Microwind tool, we analysed the power and area of both the design,and we can check the performance of both the design in table as shown below.

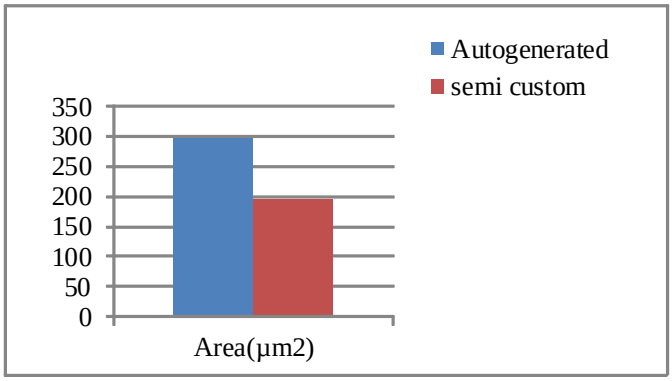
Table2. Comparison between area and power

Design	Power	Area analysis
Auto-generated	25.095µW	297.5µm2
Semi-custom	139µW	195µm2

6. CONCLUSION

Hence, from the above discussion that the area of the fully automatic layout design is 297.5µm2and power of fully automatic design is 25.095µW. The area of the fully automatic layout design is 197.5µm2and power of fully automatic design is 139µW.we concluded from the discussion that area of semi-custom layout design is reduced by 34.3 % in comparison of fully automatic design and, the speed of operation gets increased, and power of semi-custom design is reduced in future by designing a fully custom design of the circuit. Hence we can say that area in semi-custom design is better than fully automatic.

Fig.10. comparison graph of the layout designs.



REFRENCES

[1] Weste, N. H.E.; Haris, D.; Banerjee, A.(2009): Cmos vlsi design, Pearson Education Asia, Third Edition, pp 4-5.

[2] zeferinol, C.A.; Susinl, A. A. (2003): socin: a parametric and scalable network on chip" 16th symposium on integrated circuits and system design (SBCCI 2003), pp 169-174,

[3] Jaswanth, B.R.B.; Raydu, R.V.S.; Babu, K. M.; .Himaja, R.; Kumar, L.V. (2013):A design of low power buffer using using ring counter Addressing schemes. International Journal of technological Exploration and Learning Vol.2, issue.2, pp 99-103

[4] KUMAR, S. (2013): Power and Area efficient design of counter for low power VLSI system .International journal of computer science and mobile computing, vol.2, issue.6, pp 435-433

[5] Kaur, U.; Mehra, R. (2013): Low power cmos counter using gated Flip-Flop,"International Journal of engineering and advance technology, Vol.2, Issue.4, pp 796-798

[6] Wolf, W. (2007): Modern VLSI Design 3rd edn Pearson education, pp.22-27.

[7] Mahajan, A.; Mehra, R. (2015): Area Efficient Cmos layout design of ring counter. International Journal of scientific Research Engineering and Technology, pp.169-172

[8] Saini, P.; Mehra, R. (2012): Leakage Power Reduction in CMOS Design Circuits. International Journal of Computer applications, Vol.55, No.8, pp.42-48

[9] Sani, M.; Ismail, Rahman, S.; Ferdous, N.S. (2012): A Design Scheme of Toggle Operation Based Ring Counter with Efficient Clock Gating. IEEE International conference on Computational Intelligene, Modelling and Simulation, pp. 393-399

[10] Hiremath, Y.; Kulkarni, A. L.; Baligar, J. S.(2014) Design and Implementation of Synchronous 4-Bit Up Counter Using 180 nm CMOS Process Technology. International Journal of Research in Engineering and Technology (IJRET), Vol. 3, No. 5, pp. 810-815

[11] Tambat, R. V.; Lakhotiya, S. A. (2014): Design of Flip Flops for High Performance VLSI Applications using Deep Submicron CMOS Technology. International Journal of Current Engineering and Technology, Vol 4, No. 2, pp. 769-774

[12] Dastjerdi-Mottaghi, M.; Naghilou, A.; Daneshtalab, M.; Kusha, A. A.; Navabi, Z. (2006): Hot Block Ring Counter: A Low Power Synchronous Ring Counter. International Conference on Microelectronics

Authors:

Abhishek Rai: Abhishek Rai received Bachelors of Technology degree in Electronics and Communication Engineering from DAV institute of engineering and technology, Jalandhar, Punjab, India in 2015. He is pursuing Masters of engineering degree in Electronics and Communication Engineering from National Institute of Technical Teacher's Training and Research, Punjab University, Chandigarh, India. His current research interests are in VLSI .

Dr. Rajesh Mehra: Dr. Mehra is currently Head of Electronics and Communication Engineering Department at National Institute of Technical Teachers' Training & Research, Chandigarh, India. He has received his Doctor of Philosophy and Masters Degree in Electronics & Communication Engineering from Panjab University, Chandigarh, India. Dr.Mehra has completed his Bachelor of Technology from NIT, Jalandhar, India. Dr.Mehra has 22 years of Academic Experience along with 10 years of Research Experience. He has more than 450 publications in Refereed Peer Reviewed International Journals and International Conferences. More than 101 PG scholars have completed their ME thesis under his guidance. He is also guiding 03 independent PhD scholars in his research areas. He has also authored one book on PLC & SCADA. His research areas include VLSI Design, Digital Signal & Image Processing, Renewable Energy and Energy Harvesting. He is senior member IEEE and Life member ISTE.